# NCV4276B

# 400 mA Low-Drop Voltage Regulator

The NCV4276B is a 400 mA output current integrated low dropout regulator family designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with adjustable voltage versions available in 2% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and inhibit for control of the state of the output voltage. The NCV4276B is available in DPAK surface mount package. The output is stable over a wide output capacitance and ESR range. The NCV4276B has improved startup behavior during input voltage transients.

### Features

- Adjustable Voltage Version (from 2.5 V to 20 V) ±2% Output Voltage
- 400 mA Output Current
- 500 mV (max) Dropout Voltage (5.0 V Output)
- Inhibit Input
- Very Low Current Consumption
- Fault Protection
  - ♦ +45 V Peak Transient Voltage
  - ♦ −42 V Reverse Voltage
  - ♦ Short Circuit
  - ♦ Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- These are Pb−Free Devices

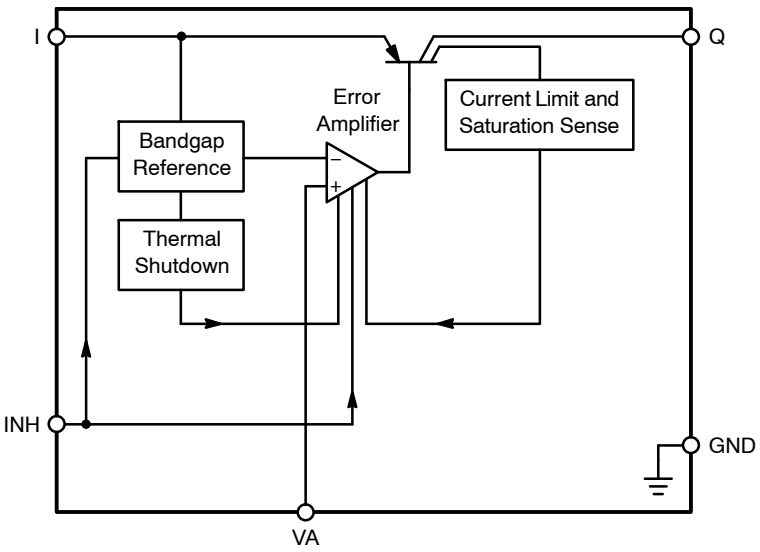
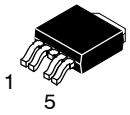



**Figure 1. Block Diagram**

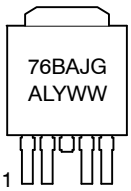
**ON Semiconductor®**

**http://onsemi.com**

**MARKING DIAGRAM**




**DPAK**
**5−PIN**
**DT SUFFIX**
**CASE 175AA**




| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Device |

*Tab is connected to Pin 3.

**ORDERING INFORMATION**

See detailed ordering and shipping information in the ordering information section on page 11 of this data sheet.

## PIN FUNCTION DESCRIPTION

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | I | Input; Battery Supply Input Voltage. |
| 2 | INH | Inhibit; Set low−to inhibit. |
| 3 | GND | Ground; Pin 3 internally connected to heatsink. |
| 4 | VA | Voltage Adjust Input; use an external voltage divider to set the output voltage |
| 5 | Q | Output: Bypass with a capacitor to GND. See Figures NO TAG to 3 and Regulator Stability Considerations section. |

## MAXIMUM RATINGS*

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage | $V_I$ | −42 | 45 | V |
| Input Peak Transient Voltage | $V_I$ | − | 45 | V |
| Inhibit INH Voltage | $V_{INH}$ | −42 | 45 | V |
| Voltage Adjust Input VA | $V_{VA}$ | −0.3 | 10 | V |
| Output Voltage | $V_Q$ | −1.0 | 40 | V |
| Ground Current | $I_q$ | − | 100 | mA |
| Input Voltage Operating Range | $V_I$ | $V_Q$ + 0.5 V or 4.5 V (Note 1) | 40 | V |
| ESD Susceptibility (Human Body Model)<br>(Machine Model) | −<br>− | 4.0<br>250 | −<br>− | kV<br>V |
| Junction Temperature | $T_J$ | −40 | 150 | °C |
| Storage Temperature | $T_{stg}$ | −50 | 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*During the voltage range which exceeds the maximum tested voltage of I, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

## LEAD TEMPERATURE SOLDERING REFLOW (Note 2)

| | | | | |
|---|---|---|---|---|
| Lead Temperature Soldering<br>Reflow (SMD styles only), Leaded, 60−150 s above 183, 30 s max at peak<br>Reflow (SMD styles only), Lead Free, 60−150 s above 217, 40 s max at peak<br>Wave Solder (through hole styles only), 12 sec max | $T_{SLD}$ | <br>−<br>−<br>− | <br>240<br>265<br>310 | °C |

## THERMAL CHARACTERISTICS

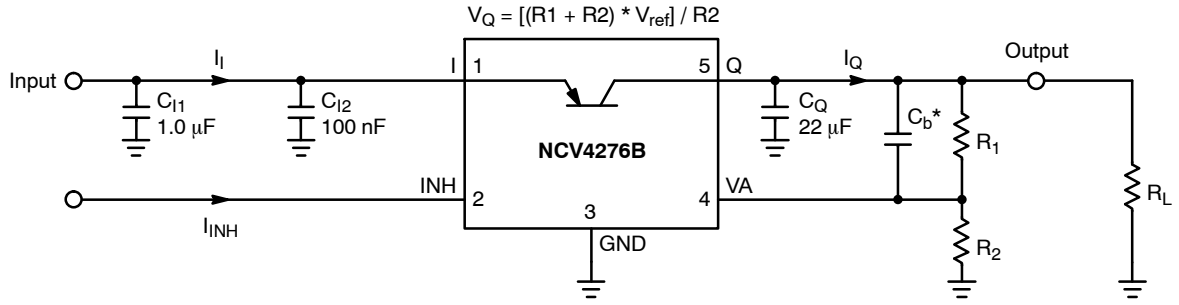
| Characteristic | Test Conditions (Typical Value) | | Unit |
|---|---|---|---|
| | **Min Pad Board** (Note 3) | **1″ Pad Board** (Note 4) | |
| Junction−to−Tab (psi−JLx, $\psi_{JLx}$) | 4.2 | 4.7 | C/W |
| Junction−to−Ambient ($R_{\theta JA}$, $\theta_{JA}$) | 100.9 | 46.8 | C/W |

1. Minimum $V_I$ = 4.5 V or ($V_Q$ + 0.5 V), whichever is higher.
2. Per IPC / JEDEC J−STD−020C.
3. 1 oz. copper, 0.26 inch$^2$ (168 mm$^2$) copper area, 0.062″ thick FR4.
4. 1 oz. copper, 1.14 inch$^2$ (736 mm$^2$) copper area, 0.062″ thick FR4.

**ELECTRICAL CHARACTERISTICS** ($V_I$ = 13.5 V; –40°C < $T_J$ < 150°C; unless otherwise noted.)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| Output Voltage | $AV_Q$ | 5.0 mA < $I_Q$ < 400 mA<br>$V_Q$+1 < $V_I$ < 40 V<br>$V_I$ > 4.5 V | –2% | – | +2% | V |
| Output Current Limitation | $I_Q$ | $V_Q$ = 90% $V_{QTYP}$ ($V_{QTYP}$ = 2.5 V) | 400 | 700 | 1100 | mA |
| Quiescent Current (Sleep Mode)<br>$I_q = I_I - I_Q$ | $I_q$ | $V_{INH}$ = 0 V | – | – | 10 | μA |
| Quiescent Current, $I_q = I_I - I_Q$ | $I_q$ | $I_Q$ = 1.0 mA | – | 130 | 200 | μA |
| Quiescent Current, $I_q = I_I - I_Q$ | $I_q$ | $I_Q$ = 250 mA | – | 10 | 15 | mA |
| Quiescent Current, $I_q = I_I - I_Q$ | $I_q$ | $I_Q$ = 400 mA | – | 25 | 35 | mA |
| Dropout Voltage | $V_{DR}$ | $I_Q$ = 250 mA, $V_{DR} = V_I - V_Q$, $V_I$ > 4.5 V | – | 250 | 500 | mV |
| Load Regulation | $\Delta V_{Q,LO}$ | $I_Q$ = 5.0 mA to 400 mA | – | 3.0 | 20 | mV |
| Line Regulation | $\Delta V_Q$ | $\Delta V_I$ = 12 V to 32 V,<br>$I_Q$ = 5.0 mA | – | 4.0 | 15 | mV |
| Power Supply Ripple Rejection | PSRR | $f_r$ = 100 Hz, $V_r$ = 0.5 $V_{PP}$ | – | 70 | – | dB |
| Temperature Output Voltage Drift | $d_{VQ/dT}$ | – | – | 0.5 | – | mV/K |
| **INHIBIT** | | | | | | |
| Inhibit Voltage, Output High | $V_{INH}$ | $V_Q \geq V_{QMIN}$ | – | 2.3 | 2.8 | V |
| Inhibit Voltage, Output Low (Off) | $V_{INH}$ | $V_Q \leq$ 0.1 V | 1.8 | 2.2 | – | V |
| Input Current | $I_{INH}$ | $V_{INH}$ = 5.0 V | 5.0 | 10 | 20 | μA |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown Temperature* | $T_{SD}$ | $I_Q$ = 5.0 mA | 150 | – | 210 | °C |

*Guaranteed by design, not tested in production.




$C_b$* – Required if usage of low ESR output capacitor $C_Q$ is demand, see Regulator Stability Considerations section

**Figure 2. Applications Circuit**

## TYPICAL PERFORMANCE CHARACTERISTICS

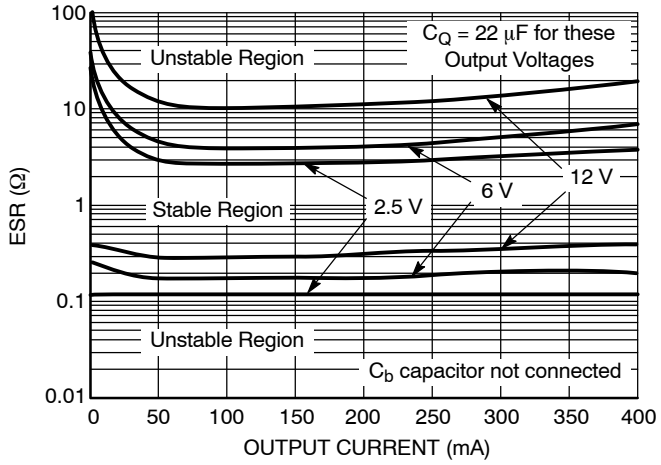



**Figure 3. Output Stability with Output Capacitor ESR**

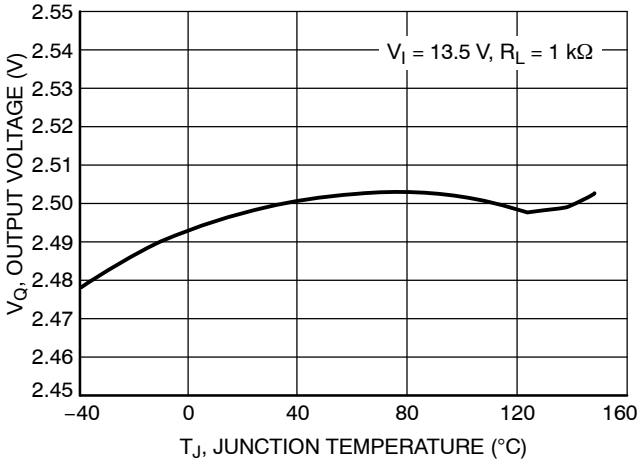



**Figure 4. Output Voltage vs. Junction Temperature**

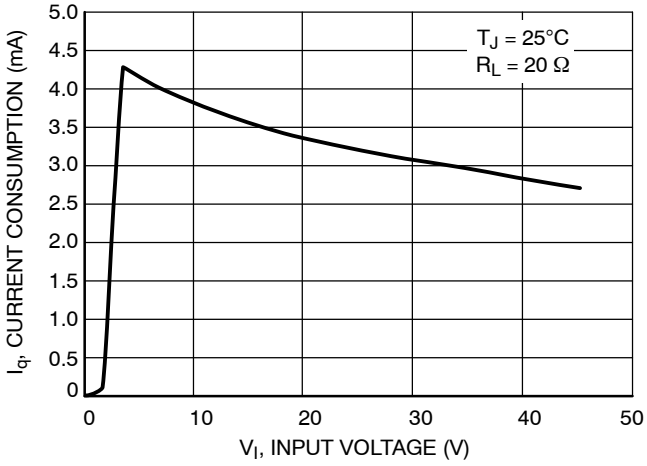



**Figure 5. Current Consumption vs. Input Voltage**

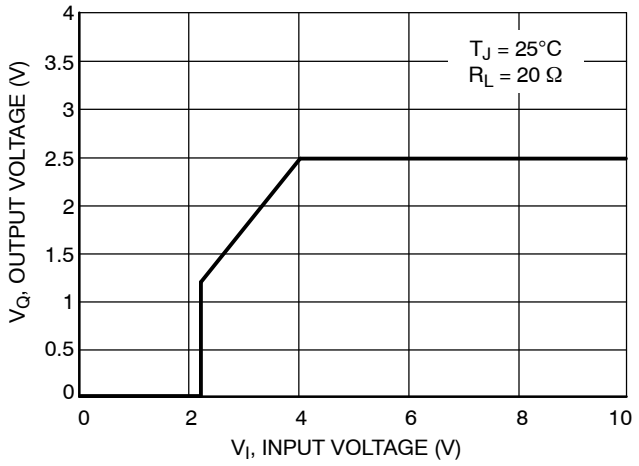



**Figure 6. Low Voltage Behavior**

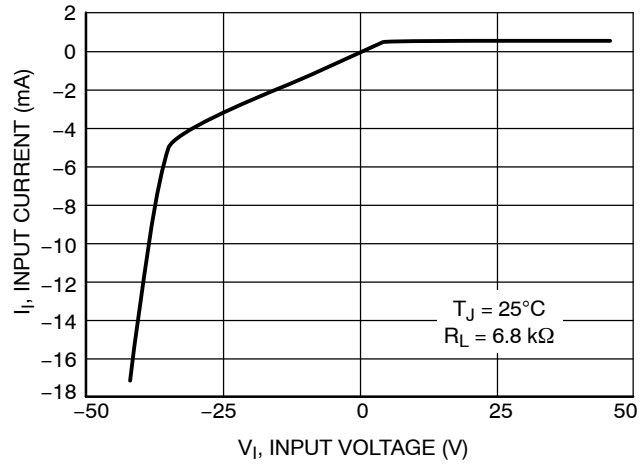



**Figure 7. High Voltage Behavior**

## TYPICAL PERFORMANCE CHARACTERISTICS

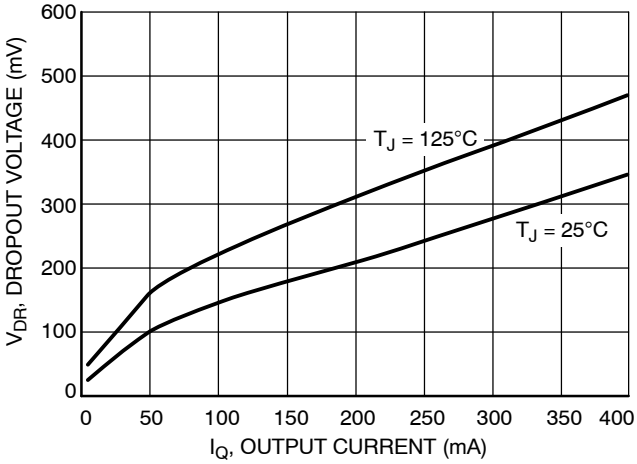



**Figure 8. Dropout Voltage vs. Output Current, Regulator Set at 5.0 V**

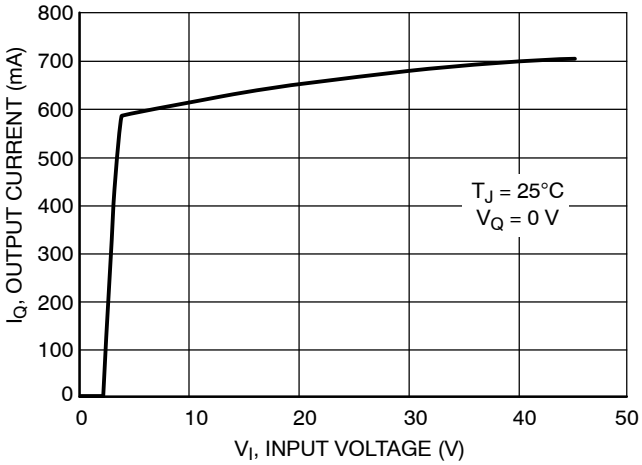



**Figure 9. Maximum Output Current vs. Input Voltage**

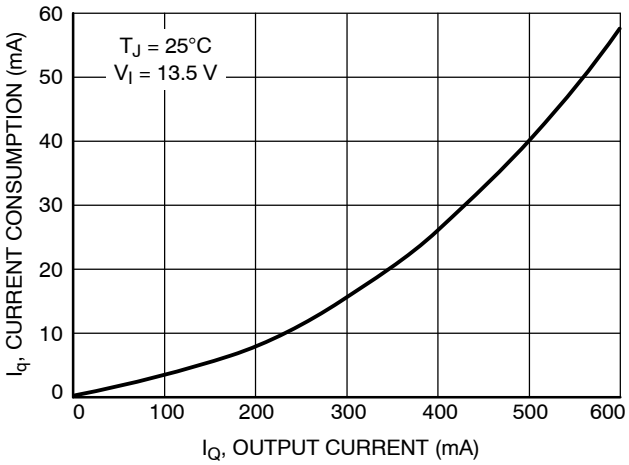



**Figure 10. Current Consumption vs. Output Current (High Load)**

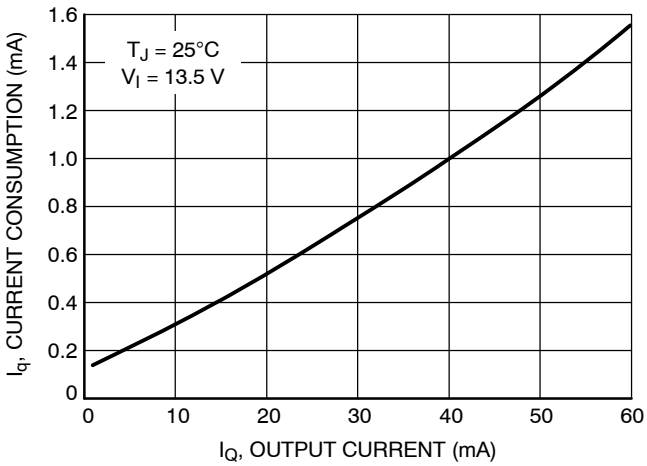



**Figure 11. Current Consumption vs. Output Current (Low Load)**

## Circuit Description

The NCV4276B is an integrated low dropout regulator that provides a regulated voltage at 400 mA to the output. It is enabled with an input to the inhibit pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 400 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

## Regulator

The error amplifier compares the reference voltage to a sample of the output voltage ($V_Q$) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized. See Figure 2, Test Circuit, for circuit element nomenclature illustration.

## Regulator Stability Considerations

The input capacitors ($C_{I1}$ and $C_{I2}$) are necessary to stabilize the input impedance to avoid voltage line influences. Using a resistor of approximately 1.0 Ω in series with $C_{I2}$ can stop potential oscillations caused by stray inductance and capacitance.

The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor $C_Q$, shown in Figure 2, should work for most applications; see also Figure 3 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 3 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

## Calculating Bypass Capacitor

If usage of low ESR ceramic capacitors is demanded, connect the bypass capacitor $C_b$ between Voltage Adjust pin and Q pin according to Applications circuit at Figure 4.

Parallel combination of bypass capacitor $C_b$ with the feedback resistor $R_1$ contributes in the device transfer function as an additional zero and affects the device loop stability, therefore its value must be optimized. Attention to the Output Capacitor value and its ESR must be paid. See also Stability in High Speed Linear LDO Regulators Application Note, AND8037/D for more information.

Optimal value of bypass capacitor is given by following expression

$$C_b = \frac{1}{2 \times \pi \times f_z \times R_1} \cdot (F)$$

where

$R_1$ = the upper feedback resistor

$f_z$ = the frequency of the zero added into the device transfer function by $R_1$ and $C_b$ external components.

Set the $R_1$ resistor according to output voltage requirement. Chose the $f_z$ with regard on the output capacitance $C_Q$, refer to the table below.

| $C_Q$ (μF) | 10 | 22 | 47 | 100 |
|---|---|---|---|---|
| $f_z$ Range (kHz) | 20 - 50 | 14 - 35 | 10 - 20 | 7 – 14 |

Ceramic capacitors and its part numbers listed bellow have been used as low ESR output capacitors $C_Q$ from the table above to define the frequency ranges of additional zero required for stability.

GRM31CR71C106KAC7 (10 μF, 16 V, X7R, 1206)

GRM32ER71C226KE18 (22 μF, 16 V, X7R, 1210)

GRM32ER61C476ME15 (47 μF, 16 V, X5R, 1210)

GRM32ER60J107ME20 (100 μF, 6.3 V, X5R, 1210)

## Inhibit Input

The inhibit pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 1.8 V, the output of the regulator will be turned off. When the voltage on the Inhibit pin is greater than 2.8 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The inhibit pin may be connected directly to the input pin to give constant enable to the output regulator.

### Setting the Output Voltage

The output voltage range can be set between 2.5 V and 20 V. This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin VA. The internal reference voltage is set to a temperature stable reference of 2.5 V.

The output voltage is calculated from the following formula. Ignoring the bias current into the VA pin:

$$V_Q = [(R1 + R2) * V_{ref}]/R2$$

Use R2 < 50 k to avoid significant voltage output errors due to VA bias current.

Connecting VA directly to Q without R1 and R2 creates an output voltage of 2.5 V.

Designers should consider the tolerance of R1 and R2 during the design phase.

The input voltage range for operation (pin 1) of the adjustable version is between ($V_Q$ + 0.5 V) and 40 V. Internal bias requirements dictate a minimum input voltage of 4.5 V. The dropout voltage for output voltages less than 4.0 V is (4.5 V − $V_Q$).

### Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 12) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad (1)$$

where

$V_{I(max)}$ is the maximum input voltage,
$V_{Q(min)}$ is the minimum output voltage,
$I_{Q(max)}$ is the maximum output current for the application,
$I_q$ is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$ less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

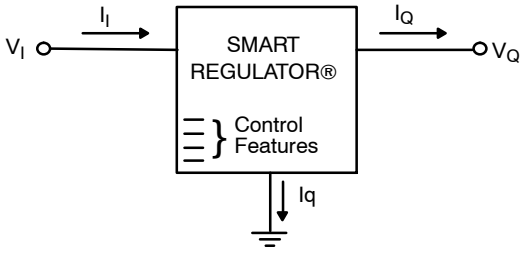



**Figure 12. Single Output Regulator with Key Performance Parameters Labeled**

### Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where

$R_{\theta JC}$ is the junction−to−case thermal resistance,
$R_{\theta CS}$ is the case−to−heatsink thermal resistance,
$R_{\theta SA}$ is the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D.

## Thermal Model

A discussion of thermal modeling is in the ON Semiconductor web site: http://www.onsemi.com/pub/collateral/BR1487−D.PDF.

**Table 1. DPAK 5−Lead Thermal RC Network Models**

| **Drain Copper Area (1 oz thick)** | | | **168 mm²** | **736 mm²** | | **168 mm²** | **736 mm²** | |
|---|---|---|---|---|---|---|---|---|
| **(SPICE Deck Format)** | | | **Cauer Network** | | | **Foster Network** | | |
| | | | 168 mm² | 736 mm² | Units | Tau | Tau | Units |
| **C_C1** | **Junction** | **GND** | 1.00E−06 | 1.00E−06 | W−s/C | 1.36E−08 | 1.361E−08 | sec |
| **C_C2** | **node1** | **GND** | 1.00E−05 | 1.00E−05 | W−s/C | 7.41E−07 | 7.411E−07 | sec |
| **C_C3** | **node2** | **GND** | 6.00E−05 | 6.00E−05 | W−s/C | 1.04E−05 | 1.029E−05 | sec |
| **C_C4** | **node3** | **GND** | 1.00E−04 | 1.00E−04 | W−s/C | 3.91E−05 | 3.737E−05 | sec |
| **C_C5** | **node4** | **GND** | 4.36E−04 | 3.64E−04 | W−s/C | 1.80E−03 | 1.376E−03 | sec |
| C_C6 | node5 | GND | 6.77E−02 | 1.92E−02 | W−s/C | 3.77E−01 | 2.851E−02 | sec |
| C_C7 | node6 | GND | 1.51E−01 | 1.27E−01 | W−s/C | 3.79E+00 | 9.475E−01 | sec |
| C_C8 | node7 | GND | 4.80E−01 | 1.018 | W−s/C | 2.65E+01 | 1.173E+01 | sec |
| C_C9 | node8 | GND | 3.740 | 2.955 | W−s/C | 8.71E+01 | 8.59E+01 | sec |
| C_C10 | node9 | GND | 10.322 | 0.438 | W−s/C | | | sec |
| | | | 168 mm² | 736 mm² | | R's | R's | |
| **R_R1** | **Junction** | **node1** | 0.015 | 0.015 | C/W | 0.0123 | 0.0123 | C/W |
| **R_R2** | **node1** | **node2** | 0.08 | 0.08 | C/W | 0.0585 | 0.0585 | C/W |
| **R_R3** | **node2** | **node3** | 0.4 | 0.4 | C/W | 0.0304 | 0.0287 | C/W |
| **R_R4** | **node3** | **node4** | 0.2 | 0.2 | C/W | 0.3997 | 0.3772 | C/W |
| **R_R5** | **node4** | **node5** | 2.97519 | 2.6171 | C/W | 3.115 | 2.68 | C/W |
| R_R6 | node5 | node6 | 8.2971 | 1.6778 | C/W | 3.571 | 1.38 | C/W |
| R_R7 | node6 | node7 | 25.9805 | 7.4246 | C/W | 12.851 | 5.92 | C/W |
| R_R8 | node7 | node8 | 46.5192 | 14.9320 | C/W | 35.471 | 7.39 | C/W |
| R_R9 | node8 | node9 | 17.7808 | 19.2560 | C/W | 46.741 | 28.94 | C/W |
| R_R10 | node9 | GND | 0.1 | 0.1758 | C/W | | | C/W |

NOTE: Bold face items represent the package without the external thermal system.

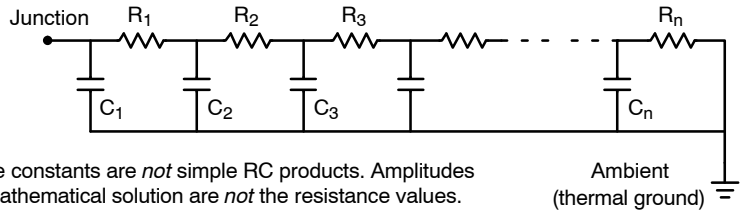



**Figure 13. Grounded Capacitor Thermal Network ("Cauer" Ladder)**

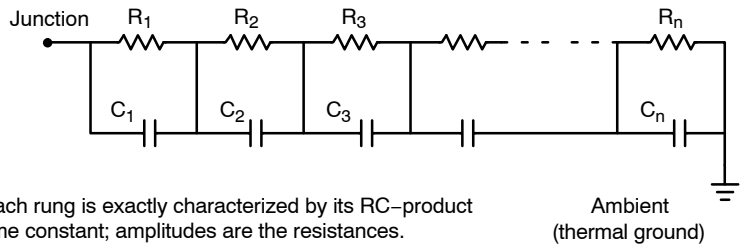



**Figure 14. Non−Grounded Capacitor Thermal Ladder ("Foster" Ladder)**

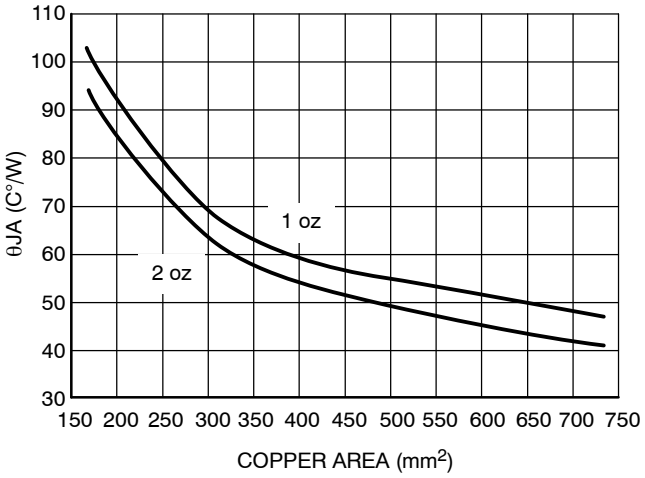



**Figure 15. θJA vs. Copper Spreader Area**

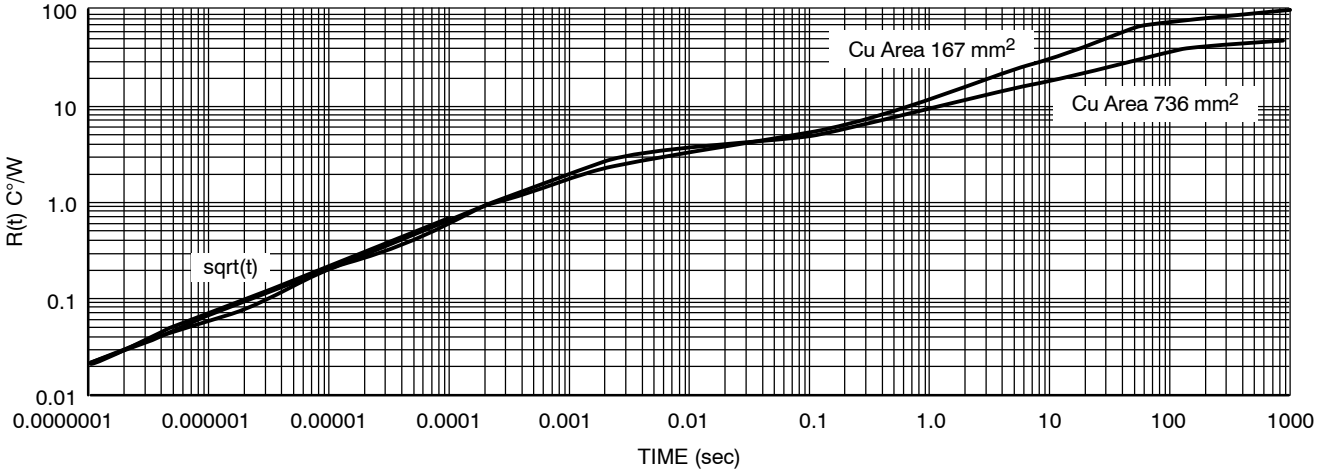



**Figure 16. Single−Pulse Heating Curves**

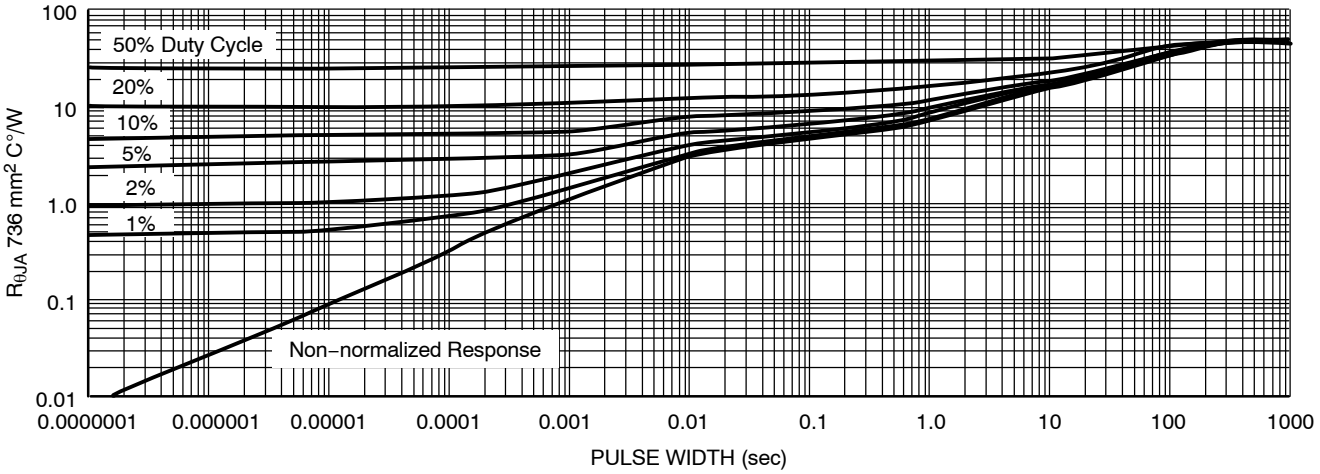



**Figure 17. Duty Cycle for 1″ Spreader Boards**

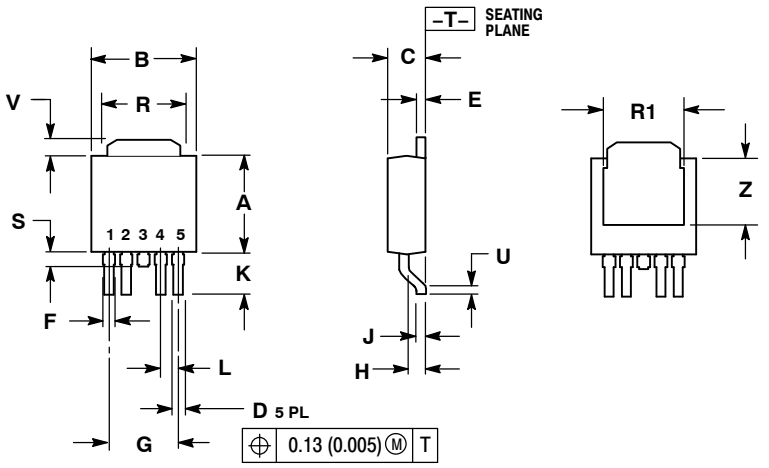
## ORDERING INFORMATION

| Device | Output Voltage Accuracy | Output Voltage | Package | Shipping† |
|---|---|---|---|---|
| NCV4276BDTADJRKG | 2% | Adjustable | DPAK, 5−Pin (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

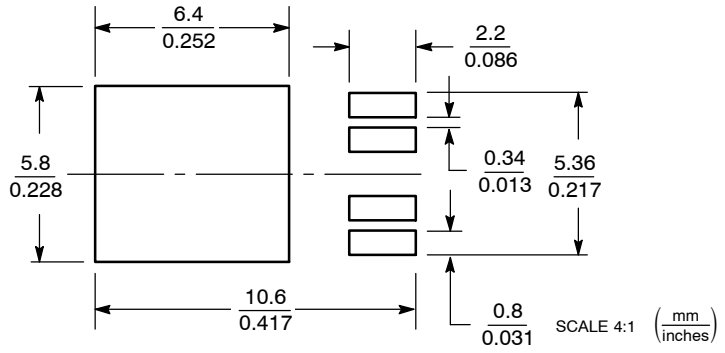
**DPAK 5, CENTER LEAD CROP**
**DT SUFFIX**
CASE 175AA−01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.020 | 0.028 | 0.51 | 0.71 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.024 | 0.032 | 0.61 | 0.81 |
| G | 0.180 BSC | | 4.56 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.045 BSC | | 1.14 BSC | |
| R | 0.170 | 0.190 | 4.32 | 4.83 |
| R1 | 0.185 | 0.210 | 4.70 | 5.33 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | −−− | 0.51 | −−− |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | 0.170 | 3.93 | 4.32 |

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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