

## 70-V Fault-Protected RS-485 Transceivers

#### **FEATURES**

- Bus-Pin Fault Protection to > ±70 V
- Operation With 3.3-V to 5-V Supply Range
- ±16 kV HBM Protection on Bus Pins
- Reduced Unit Load for up to 320 Nodes
- Failsafe Receiver for Open-Circuit,
   Short-Circuit and Idle-Bus Conditions
- Low Power Consumption
  - Low Standby Supply Current, 1 μA Max
  - I<sub>CC</sub> 4 mA Quiescent During Operation
- Pin-Compatible With Industry-Standard SN75176

 Signaling Rates of 115 kbps, 1 Mbps, and up to 10 Mbps

#### **APPLICATIONS**

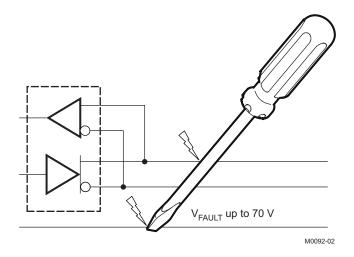
- HVAC Networks
- Security Electronics
- Building Automation
- Telecomm Equipment
- Motion Control
- Industrial Networks

### **DESCRIPTION**

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. The internal current-limit circuits allow fault survivability without causing the high bus currents that otherwise might damage external components or power supplies. They are also robust to ESD events, with high levels of protection to the JEDEC or IEC human-body-model specification.

These devices combine a differential driver and a differential receiver, which operate from a single power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. This port features a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from –40°C to 125°C. These devices are pin-compatible with the industry-standard SN75176 transceiver, making them drop-in upgrades in most systems.

These devices are fully compliant with ANSI TIA/EIA 485-A with a 5-V supply and can operate with a 3.3-V supply with reduced driver output voltage for low-power applications. For applications where operation is required over an extended common-mode voltage range, see the SN65HVD1785 (SLLS872) data sheet.



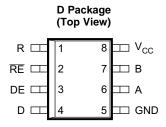


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

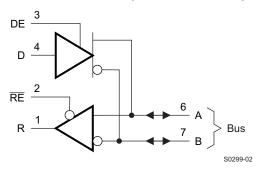




These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



## **LOGIC DIAGRAM (POSITIVE LOGIC)**



### **DEVICE INFORMATION**

### **DRIVER FUNCTION TABLE**

Input	Enable	Outp	uts	Driver State
D	DE	Α	В	
Н	Н	Н	L	Actively drive bus High
L	Н	L	Н	Actively drive bus Low
Х	L	Z	Z	Driver disabled <sup>(1)</sup>
Х	OPEN	Z	Z	Driver disabled by default (1)
OPEN	Н	Н	L	Actively drive bus High by default

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.

#### **RECEIVER FUNCTION TABLE**

Differential Input	Enable	Output	Receiver State
$V_{ID} = V_A - V_B$	RE	R	
$V_{IT+} < V_{ID}$	L	Н	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	Н	Z	Receiver disabled <sup>(1)</sup>
X	OPEN	Z	Receiver disabled by default (1)
Open-circuit bus	L	Н	Fail-safe high output
Short-circuit bus	L	Н	Fail-safe high output
Idle (terminated) bus	L	Н	Fail-safe high output

(1) When both the driver and receiver are disabled, the device enters a low-power standby mode.



## ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
$V_{CC}$	Supply voltage	-0.5 to 7	V
	Voltage range at A and B inputs	-70 to 70	V
	Input voltage range at any logic pin	-0.3 to V <sub>CC</sub> + 0.3	V
	Voltage input range, transient pulse, A and B, through 100 $\Omega$	-70 to 70	V
	Receiver output current	-24 to 24	mA
T <sub>J</sub>	Junction temperature	170	°C
	Continuous total power dissipation	See Dissipation Rating Table	
	IEC 60749-26 ESD (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), bus terminals and GND	±16	kV
	JEDEC Standard 22, Test Method A114 (human-body model), all pins	±4	kV
	JEDEC Standard 22, Test Method C101 (charged-device model), all pins	±2	kV
	JEDEC Standard 22, Test Method A115 (machine model), all pins	±400	V

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### PACKAGE DISSIPATION RATINGS

PACKAGE <sup>(1)</sup>	JEDEC THERMAL MODEL	THERMAL T <sub>A</sub> < 25°C DERATING FACTOR		T <sub>A</sub> = 85°C RATING	T <sub>A</sub> = 105°C RATING	T <sub>A</sub> = 125°C RATING (3.3 V ONLY)	
SOIC (D) 9 pin	High-K	905 mW	7.25 mW/°C	470 mW	325 mW	180 mW	
SOIC (D) 8-pin	Low-K	516 mW	4.1 mW/°C	268 mW	186 mW	103 mW	

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

#### RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT	
$V_{CC}$	Supply voltage		3.15	5	5.5	V	
VI	Input voltage at any bus terminal (separately	or common mode) <sup>(1)</sup>	-7		12	V	
$V_{IH}$	High-level input voltage (driver, driver enable	e, and receiver enable inputs)	2		$V_{CC}$	V	
$V_{IL}$	Low-level input voltage (driver, driver enable	e, and receiver enable inputs)	0		0.8	V	
$V_{\text{ID}}$	Differential input voltage	-12		12	V		
	Output current, driver	-60		60	mA		
IO	Output current, receiver		e) <sup>(1)</sup>	8	mA		
$R_L$	Differential load resistance	54	60		Ω		
$C_L$	Differential load capacitance			50		pF	
		HVD1780			115	kbps	
1/t <sub>UI</sub>	Signaling rate	HVD1781			1	Mana	
		HVD1782			1 10	Mbps	
т	Operating free-air temperature (See	5-V supply	-40		105	°C	
T <sub>A</sub>	application section for thermal information)	3.3-V supply	-40		125		
TJ	Junction temperature		-40		150	°C	

<sup>(1)</sup> By convention, the least positive (most negative) limit is designated as minimum in this data sheet.



## **ELECTRICAL CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS		MIN	TYP	MAX	UNIT
		$R_L = 60 \Omega, 4.75 V \le V_C$		T <sub>A</sub> < 85°C	1.5			
		on each output to –7 V to 12 V Figure 1		T <sub>A</sub> < 125°C	1.4			
		$ R_L = 54 \Omega,$ $ 4.75 \text{ V} \le \text{V}_{CC} \le 5.25 \text{ V}$		T <sub>A</sub> < 85°C	1.7	2		
V <sub>OD</sub>	Driver differential output voltage magnitude			T <sub>A</sub> < 125°C	1.5			٧
		$R_L = 54 \Omega,$ 3.15 V $\leq$ V <sub>CC</sub> $\leq$ 3.45 V			0.8	1		
		R <sub>L</sub> = 100 Ω,		T <sub>A</sub> < 85°C	2.2	2.5		
		$4.75 \text{ V} \le \text{V}_{CC} \le 5.25 \text{ V}$		T <sub>A</sub> < 125°C	2			
$\Delta  V_{OD} $	Change in magnitude of driver differential output voltage	R <sub>L</sub> = 54 Ω			-50	0	50	mV
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage				1	V <sub>CC</sub> /2	3	V
$\Delta V_{OC}$	Change in differential driver output common-mode voltage				-50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω loa See Figure 2	d resistor	S,		500		mV
C <sub>OD</sub>	Differential output capacitance					23		pF
$V_{\text{IT+}}$	Positive-going receiver differential input voltage threshold					-100	-35	
$V_{\text{IT-}}$	Negative-going receiver differential input voltage threshold		-180	-150		mV		
$V_{HYS}$	Receiver differential input voltage threshold hysteresis $(V_{IT+} - V_{IT-})$				30	50		
$V_{OH}$	Receiver high-level output voltage	$I_{OH} = -8 \text{ mA}$			2.4	V <sub>CC</sub> – 0.3		V
$V_{OL}$	Receiver low-level output voltage	I <sub>OL</sub> = 8 mA	T <sub>A</sub> < 85°			0.2	0.4	V
VOL	· · · · ·	101 = 0 111/1	$T_A < 125$	°C		·	0.5	•
$I_{I(LOGIC)}$	Driver input, driver enable, and receiver enable input current				<b>–</b> 50		50	μΑ
l <sub>OZ</sub>	Receiver output high-impedance current	$V_O = 0 \text{ V or } V_{CC}, \overline{RE}$ at	t V <sub>CC</sub>		-1		1	μΑ
los	Driver short-circuit output current			,	-200		200	mA
I <sub>I(BUS)</sub>	Bus input current (disabled driver)	V <sub>CC</sub> = 3.15 to 5.5 V or	V <sub>I</sub> = 12 \			75	100	μΑ
1(000)		$V_{CC} = 0 \text{ V}, \text{ DE at } 0 \text{ V}$	V <sub>I</sub> = −7 \		-60	-40		r-
		Driver and receiver enabled	DE = V <sub>C</sub> RE = GN no load	c, ID,		4	6	
		Driver enabled, receiver disabled	DE = V <sub>C</sub> RE = V <sub>C</sub> no load			3	5	mA
I <sub>CC</sub>	Supply current (quiescent)	Driver disabled, receiver enabled	disabled, DE = GND,			2	4	
	,,	Driver and receiver disabled, standby		n, C <sup>,</sup> T <sub>A</sub> < 85°C		0.15	1	μА
		mode DE = D = 0 RE =		٦,			12	μπ
	Supply current (dynamic)	See the Typical Cha	aracteristic	s section				



## **SWITCHING CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CO	TEST CONDITIONS			MAX	UNIT	
DRIVER (HVI	D1780)	T.	1					
t <sub>r</sub> , t <sub>f</sub>	Driver differential output rise/fall time			0.4	1.7	2.6	μs	
t <sub>PHL</sub> , t <sub>PLH</sub>	Driver propagation delay	$R_L = 54 \Omega, C_L = 50$	nF See Figure 3		0.8	2	μs	
t <sub>SK(P)</sub>	Driver differential output pulse skew,  t <sub>PHL</sub> - t <sub>PLH</sub>	1\(\( = 04 \)2, \(\text{O} \( = 00 \)	11 = 34 22, 0[ = 30 pr , 000 r iguio 3			250	ns	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Driver disable time						μs	
	Driver exchiptions	Receiver enabled	Receiver enabled See Figure 4 and Figure 5		0.2	3		
t <sub>PZH</sub> , t <sub>PZL</sub>	Driver enable time	Receiver disabled	- I iguic o		3	12	μs	
DRIVER (HVI	01781)	T.				'		
t <sub>r</sub> , t <sub>f</sub>	Driver differential output rise/fall time			50		300	ns	
t <sub>PHL</sub> , t <sub>PLH</sub>	Driver propagation delay	R 54 O. C 50	nE See Figure 3			200	ns	
t <sub>SK(P)</sub>	Driver differential output pulse skew,  t <sub>PHL</sub> - t <sub>PLH</sub>	T( = 54 12, O( = 50	$R_L = 54 \Omega$ , $C_L = 50 pF$ , See Figure 3			25	ns	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Driver disable time					3	μs	
	Driver exchiptions	Receiver enabled	See Figure 4 and Figure 5			300	ns	
t <sub>PZH</sub> , t <sub>PZL</sub>	Driver enable time	Receiver disabled	- Tigulo 0			10	μs	
DRIVER (HVI	01782)					,		
			All V <sub>CC</sub> and Temp			50		
$t_r$ , $t_f$	Driver differential output rise/fall time	$R_L = 54 \Omega$	$V_{CC} > 4.5V$ and $T < 105^{\circ}C$			30	ns	
t <sub>PHL</sub> , t <sub>PLH</sub>	Driver propagation delay	C <sub>L</sub> = 50 pF				50	ns	
t <sub>SK(P)</sub>	Driver differential output pulse skew,  t <sub>PHL</sub> - t <sub>PLH</sub>		See Figure 3			10	ns	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Driver disable time					3	μs	
	Deliver weekle Con-	Receiver enabled	See Figure 4 and Figure 5			300	ns	
$t_{PZH}$ , $t_{PZL}$	Driver enable time	Receiver disabled	Tiguic 3			9	μs	
RECEIVER (A	ALL DEVICES UNLESS OTHERWISE NOT	ED)				'		
t <sub>r</sub> , t <sub>f</sub>	Receiver output rise/fall time		All devices		4	15	ns	
t <sub>PHL</sub> , t <sub>PLH</sub>	Receiver propagation delay time		HVD1780, HVD1781		100	200	ns	
THE TEN	, , ,	C <sub>L</sub> = 15 pF, See Figure 6	HVD1782			80		
t <sub>SK(P)</sub>	Receiver output pulse skew,	See Figure 0	HVD1780, HVD1781		6	20	ns	
- : - \( \)	t <sub>PHL</sub> — t <sub>PLH</sub>		HVD1782			5		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Receiver disable time	Driver enabled, See	e Figure 7		15	100	ns	
t <sub>PZL(1)</sub> , t <sub>PZH(1)</sub>	Pagaiyar anabla tima	Driver enabled, See	Driver enabled, See Figure 7			300	ns	
$t_{PZL(2)}, t_{PZH(2)}$	Receiver enable time	Driver disabled, See	Driver disabled, See Figure 8				μs	

### THERMAL INFORMATION

PARAMETER		TEST CONDITIONS	VALUE	UNIT		
	SOIC-8	JEDEC high-K model	138			
	SOIC-8	JEDIC low-K model	242			
D. Jungtion to ambient they well registered (no sinfley)	DIP-8	JEDEC high-K model	59	°C/W		
$R_{ heta JA}$ Junction-to-ambient thermal resistance (no airflow	DIP-6	JEDIC low-K model	128	*C/VV		
	SOIC-14	JEDEC high-K model	95			
	SOIC-14	JEDIC low-K model	168			
	SOIC-8		62			
R <sub>0JB</sub> Junction-to-board thermal resistance	DIP-8		39	°C/W		
	SOIC-14		40			
	SOIC-8		61			
R <sub>BJC</sub> Junction-to-case thermal resistance	DIP-8		61	°C/W		
	SOIC-14		44			
		$V_{CC}=3.6V, T_J=150^{\circ}C, R_L=300\Omega,$ $C_L=50$ pF (driver), $C_L=15$ pF (receiver) 3.3-V supply, unterminated <sup>(1)</sup>	75			
		$V_{CC} = 3.6V$ , $T_J = 150^{\circ}C$ , $R_L = 100 \Omega$ , $C_L = 50 \text{ pF}$ (driver), $C_L = 15 \text{ pF}$ (receiver) 3.3-V supply, RS-422 load <sup>(1)</sup>	95			
		$V_{CC} = 3.6V$ , $T_J = 150^{\circ}C$ , $R_L = 54 \Omega$ , $C_L = 50  \text{pF}$ (driver), $C_L = 15  \text{pF}$ (receiver) 3.3-V supply, RS-485 load <sup>(1)</sup>	115			
P <sub>D</sub> Power dissipation		$V_{CC}$ = 5.5V, $T_J$ = 150°C, $R_L$ = 300 $\Omega$ , $C_L$ = 50 pF (driver), $C_L$ = 15 pF (receiver) 5-V supply, unterminated <sup>(1)</sup>	290	mW		
		$V_{CC} = 5.5V$ , $T_J = 150^{\circ}C$ , $R_L = 100 \Omega$ , $C_L = 50 \text{ pF}$ (driver), $C_L = 15 \text{ pF}$ (receiver) 5-V supply, RS-422 load <sup>(1)</sup>	320			
		$V_{CC}$ = 5.5V, $T_J$ = 150°C, $R_L$ = 54 $\Omega$ , $C_L$ = 50 pF (driver), $C_L$ = 15 pF (receiver) 5-V supply, RS-485 load <sup>(1)</sup>	400			
T <sub>SD</sub> Thermal-shutdown junction temperature			170	°C		

<sup>(1)</sup> Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: 1 Mbps.

#### PARAMETER MEASUREMENT INFORMATION

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50  $\Omega$ .

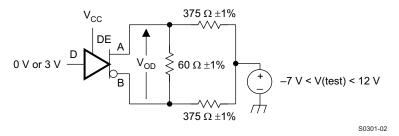


Figure 1. Measurement of Driver Differential Output Voltage With Common-Mode Load



## PARAMETER MEASUREMENT INFORMATION (continued)

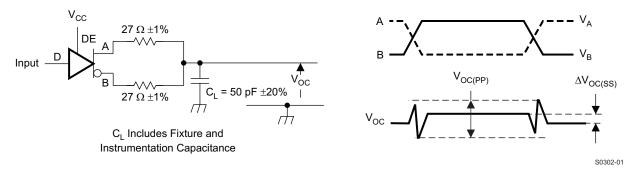


Figure 2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

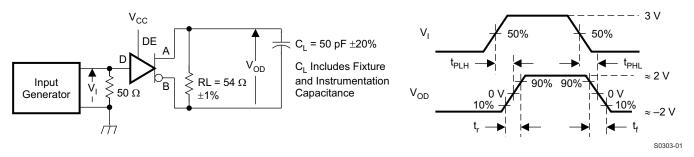
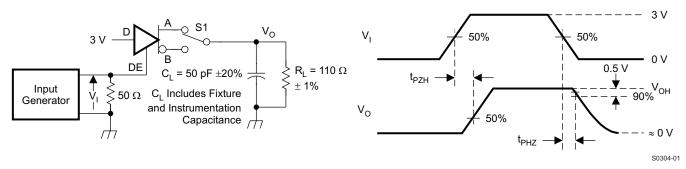
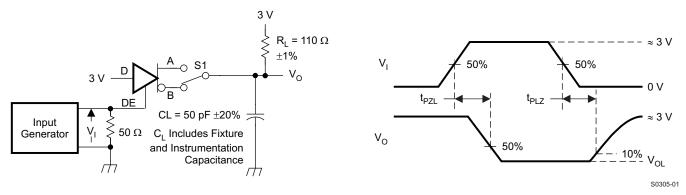


Figure 3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 4. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

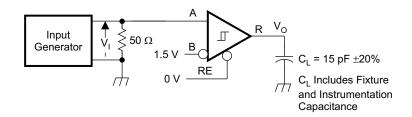


NOTE: D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 5. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load



## PARAMETER MEASUREMENT INFORMATION (continued)



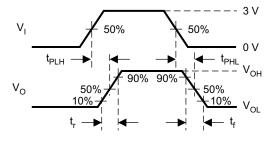


Figure 6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

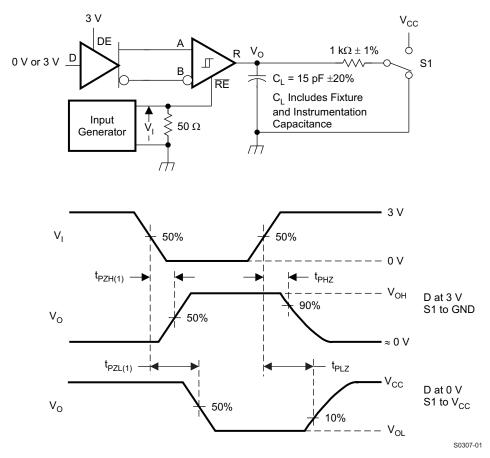


Figure 7. Measurement of Receiver Enable/Disable Times With Driver Enabled

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## PARAMETER MEASUREMENT INFORMATION (continued)

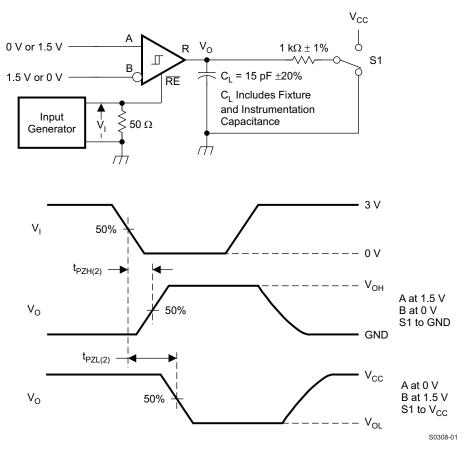
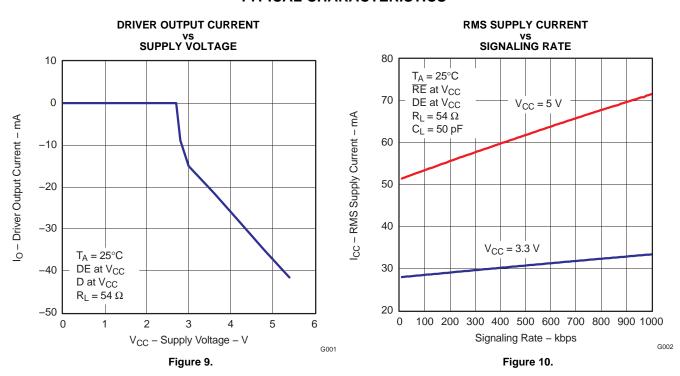
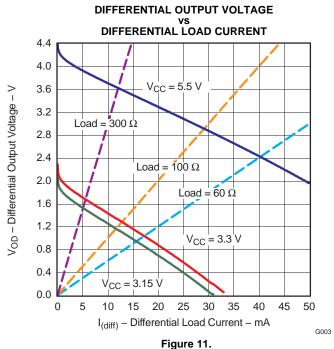


Figure 8. Measurement of Receiver Enable Times With Driver Disabled



## **TYPICAL CHARACTERISTICS**









7-Aug-2008

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65HVD1781D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1781DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1781DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1781DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

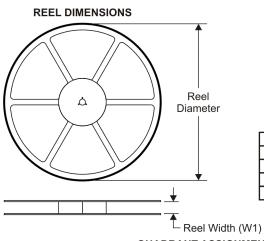
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

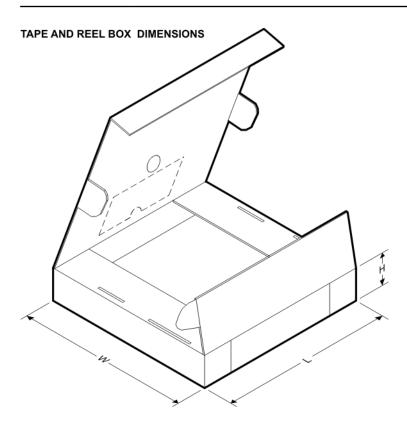
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1781DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1





#### \*All dimensions are nominal

ĺ	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
	SN65HVD1781DR	SOIC	D	8	2500	346.0	346.0	29.0	

# D (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.



#### **IMPORTANT NOTICE**

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